REMARKS

By the foregoing amendment, claims 1, 9, 17, 25, 33, and 39 have been amended as requested by the Examiner, and to more clearly distinguish the claims from the one reference cited by the Examiner in the most recent rejection. Marked-up versions of the amended claims are provided in the attached Appendix.

In the Office Action, claims 1-44 were rejected under 35 U.S.C. § 103 as being obvious over Shinagawa (U.S. Patent No. 5,126,541).

With regard to the § 103(a) rejections of the independent claims 1, 19, 17, 25, 33 and 39, each of these claims have been amended to make clear that, in contrast to the Shinagawa reference, certain programming instructions loaded at the time of manufacture are not operational until subsequent storing of an address table (with memory addresses of at least one of said programming instructions) at the time of personalization. These claims further require: (1) the manufacture of an IC card including storage of programming instructions, but not including storage of an address table with memory addresses of at least one of the programming instructions; and (2) the aforementioned address table is stored on the card during personalization of the card. One benefit is increased security by insuring that certain card use is prevented until the card is enabled at the personalization step with an address table to reference a particular set of loaded programming instructions or primitives (see, e.g., page 5, ¶ 00012).

Applicants have carefully reviewed the Shinagawa reference, particularly the sections cited on page 3 of the Office Action (col. 3, ln. 50 - col. 4, ln. 21; col. 5, lines 12-25; Figure 5 and col. 7, ln. 60 - col. 8, ln. 3), and are unable to find any mention or suggestion of an IC card which is manufactured with programming instructions which are

not operational until subsequent loading of an address table at time of personalization. In particular, there is only one program stored on the Shinagawa card during the manufacturing process: the system program, a/k/a the basic processing program. *See* col. 3, lns. 50-52. It is apparent from the reference that the system program is immediately operational after the card is manufactured, because the manufactured card is ready to receive the application program during the issuing process. *See* col. 3, lns. 52-58 and 61-64. It is therefore clear that, once the card has been manufactured, the programming instructions included in the system program are operational. In other words, the Shinagawa reference clearly fails to disclose or suggest the present claimed invention of claims 1, 9, 17, 25, 33, and 39.

In addition, unlike the present claimed invention, the Shinagawa reference provides no motivation for providing a card system with the above-described features. As is stated on page 11, ¶00030 of the specification, a benefit of the present invention is that it allows the system to use a card "despite an outdated codelet or primitive which may have been permanently placed in the card at the time of manufacture." In contrast, the methods taught in the cited reference are for the purposes of debugging, developing, and evaluating applications to be executed on IC Cards (*see* col. 2, lns. 25-35; col. 4, lns. 40-57; col. 5, ln. 66 - col. 6, ln. 1; and col. 6, lns. 6 - 48), and are completely unrelated to enabling the use of a card despite an outdated codelet or primitive remaining on the card. Shinagawa makes no mention or suggestion of outdated codelets or primitives, much less whether it would be beneficial to use a card having such outdated codelets or primitives. Accordingly, it is clear that the present claimed invention is neither anticipated nor

rendered obvious by Shinagawa, and at least independent claims 1, 9, 17, 25, 33, and 39 are in condition for allowance.

With regard to the rejected dependent claims, applicants submit that these claims are allowable as well, at least for the reasons stated above. Dependent claims 2, 5, 10, 13, 18, 21, 27, 29, 35 and 41 recite the further limitation of programming instructions which comprise at least one primitive. Applicants are unable to find any mention of primitives anywhere in the cited reference, Shinagawa, and in fact, the section cited on page 3 of the Office Action (col. 5, lines 16-25) merely describes a "debugger program [which] sets to [a] data memory ... address information items and the like" to be used in a data output section, a program initiate section, and a program stop section. The data output section, the program initiate section, and the program stop section are then initiated by generating operation enable signals. Shinagawa does not state or even suggest that the aforementioned sections are primitives. As is stated on page 3, ¶ 0006 of the present application, "Primitives are written in native language (i.e. assembler language) so that they can be executed very quickly and minimal interpretation of the instructions is necessary for execution." Shinagawa fails to provide any such description or even use the word "primitive." Furthermore, there is nothing in Shinagawa which would suggest that the data output section, the program initiate section, or the program stop section are, or should be, primitives. It is therefore clear that the additional limitations recited in claims 2, 5, 10, 13, 18, 21, 27, 29, 35 and 41 of the present invention are neither anticipated nor rendered obvious by the cited reference. Accordingly, because these claims depend from allowable independent claims, and recite

further novel and non-obvious limitations, claims 2, 5, 10, 13, 18, 21, 27, 29, 35 and 41 should be allowed.

Dependent claims 3, 6, 11, 14, 19, 22, 28, 30, 36 and 42 recite the further limitation of programming instructions which comprise at least one codelet. Applicants are unable to find any mention of codelets anywhere in Shinagawa, and in particular, the figure and section cited on page 3 of the Office Action (figure 5 and col. 5, lines 12-16) have nothing to do with storing codelets in the memory of a card. The cited section of Shinagawa merely discusses switching a mode of a card to a "development mode," and initiating a debugger program. Furthermore, Applicants are unable to find any indication, anywhere in the cited reference, that storing a codelet would be useful for switching a card to a development mode and initiating a debugger program. It is therefore clear that the cited reference neither teaches nor renders obvious the additional limitations recited in claims 3, 6, 11, 14, 19, 22, 28, 30, 36 and 42. Accordingly, because these dependent claims depend from allowable base claims, and recite further novel and non-obvious limitations, claims 3, 6, 11, 14, 19, 22, 28, 30, 36 and 42 should be allowed.

Furthermore, dependent claims 7, 15, 23, 31 and 37 recite the additional limitation of an address table which comprises a listing of names and addresses of primitives; and dependent claims 8, 16, 24, 32 and 38 recite the additional limitation of an address table which comprises a listing of names and addresses of codelets. In contrast, the cited reference fails to teach such limitations. In particular, Applicants are unable to find any mention or suggestion, anywhere in the cited reference, of the storage of the name of a programming instruction in an address table. As for Figure 1 of Shinagawa, which is cited on page 3 of the Office Action, this drawing fails to disclose

any name associated with programming instructions stored in a table. In addition, Shinagawa does not disclose or suggest any reason why the storage of a name of a set of programming instructions would be of any use or benefit for the mode-switching and debugging techniques discussed in the reference. It is therefore clear that the cited reference fails to disclose or render obvious the additional limitations of present claims 7, 8, 15, 16, 23, 24, 31, 32, 37 and 38. Accordingly, because each of these claims depends from allowable claims and recites further novel and non-obvious limitations, claims 7, 8, 15, 16, 23, 24, 31, 32, 37 and 38 are also allowable.

Dependent claims 26, 34, and 40 include the following features: (1) the storage of additional programming instructions corresponding to updated versions of previously stored or existing programming instructions; and (2) inserting addresses in an address table by overwriting existing addresses with the addresses of the corresponding updated programming instructions. Applicants are unable to find any such features anywhere in Shinagawa, the cited reference. In particular, the section cited on page 3 of the Office Action (col. 4, lines 44-48) merely refers to the loading of debug processing data including information to specify an initiating position or an execution start address of an application program. No mention is made of either: (1) updated versions of previously stored programming instructions, or (2) overwriting existing addresses with addresses of the corresponding updated programming instructions. In fact, there is nothing in Shinagawa which would provide any motivation for such features, and accordingly, the additional subject matter recited in claims 26, 34, and 40 cannot be either anticipated or rendered obvious by the cited reference. Moreover, although it may be "common practice in the art to meet customers' needs and expectation" as the

Examiner suggests, the method and system claimed by applicants is nowhere disclosed or suggested by the prior art. Therefore, because claims 26, 34, and 40 depend from allowable claims, and recite further novel and non-obvious subject matter, the present invention according to claims 26, 34, and 40 is also patentable over Shinagawa.

With regard to the § 103(a) rejections of independent claims 43 and 44 over Shinagawa, each of these claims further recite the following features: (1) manufacturing an IC card and storing at the time of manufacture in the IC card a first set of programming instructions having a first address, without an address table with a second memory address of a second set of programming instructions; (2) storing in the IC card the second set of programming instructions; and (3) storing in the IC card, at a time of personalization, the address table with the second memory address, wherein after the time of personalization, the first set of programming instructions is rendered inaccessible to the operating system.

Applicants have carefully reviewed the Shinagawa reference, particularly the sections cited on page 3 of the Office Action (col. 3, line 50 - col. 4, line 21; and col. 7, line 60 - col. 8, line 3), and are unable to find any mention or suggestion of the aforementioned features in the cited reference. Moreover, as is discussed above with respect to claims 1, 9, and 17, the purposes of the Shinagawa system are debugging, developing, and evaluating applications to be executed on IC cards (*see* col. 2, lns. 25-35; col. 4, lns. 40-57; col. 5, ln. 66 - col. 6, ln. 1; and col. 6, lns. 6-48), and the cited reference therefore provides no motivation for employing the aforementioned features of the present invention according to claims 43 and 44. For example, there is no mention or suggestion of rendering any set of programming instructions inaccessible after

personalization of the Shinagawa card, nor does the reference provide any reason for such a feature.

In addition, applicants point out that the same reference — Shinagawa — was also the sole reference at issue in the parent application, Serial No. 09/162,605, now U.S. Patent No. 6,357,665. Applicants therefore respectfully refer the Examiner to the following language in his reasons for allowance set forth on page 2 of the July 30, 2001 Notice of Allowability in the parent application:

> The applicant teaches a multiple application card system having a manufacturing process wherein the manufacturing process includes storing a first set of programming instructions having a first address, without an address table and storing a second set of programming instructions having a second address and an address table, wherein the first programming instructions are not accessible by the operating system. These limitations in conjunction with other limitations of the independent and dependent claims were not shown by the prior art.

Applicants respectfully request that the Examiner consider the features recited in currently pending claims 43 and 44 in view of the above-cited reasons for allowance in the parent case. It is believed that the above-cited reasons for allowance make it even more apparent that claims 43 and 44 are allowable over Shinagawa.

Applicants submit that the foregoing discussion of claims 43 and 44 demonstrates that these claims recite subject matter which is novel and non-obvious over the Shinagawa reference, and that these claims should therefore be allowed.

Accordingly, in light of the foregoing discussion, it is submitted that claims 1-44, all of the pending claims, are in condition for allowance. Favorable reconsideration of these claims is therefore respectfully requested.

Respectfully submitted,

Dated: May 14, 2003

Robert C. Scheinfeld
Patent Office Reg. No. 31,300

BAKER BOTTS L.L.P.
30 Rockefeller Plaza
New York, New York 10112-4498
Attorney for Applicants
(212) 408-2512

APPENDIX A

VERSIONS WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 1, 9, 17, 25, 33, and 39 have been amended as follows:

1. (Twice Amended) A secure multiple application card system including an IC card comprising a microprocessor, a read-only memory and an electrically erasable programmable read only memory, said system comprising:

means for manufacturing said IC card and for storing at the time of manufacture in said read-only memory an operating system and programming instructions without an address table with memory addresses of at least one of said programming instructions, said programming instructions not being operational until subsequent storing of said address table at the time of personalization; and

means for personalizing said IC card after said manufacturing step and for storing at the time of personalization in said electrically erasable programmable read only memory said address table with memory addresses of at least one of said programming instructions,

wherein the operating system will only access [those] the programming instructions in accordance with the addresses indicated in the address table.

9. (Twice Amended) A process for providing a secure multiple application card system including an IC card comprising a microprocessor, a read-only memory and an electrically erasable programmable read only memory, said process comprising the steps of:

manufacturing said IC card and storing at the time of manufacture in said read-only memory an operating system and programming instructions without an address table with memory addresses of at least one of said programming instructions, said programming instructions not being operational until subsequent storing of said address table at the time of personalization; and

personalizing said IC card after said time of manufacture by storing in said electrically erasable programmable read only memory said address table with memory addresses of at least one of said programming instructions,

wherein the operating system will only access [those] the programming instructions in accordance with the addresses indicated in the address table.

17. (Twice Amended) A process for providing a secure multiple application card comprising a microprocessor, a first memory and a second memory, said process comprising the steps of:

manufacturing said card and storing at the time of manufacture in said first memory an operating system and programming instructions without an address table with memory addresses of at least one of said programming instructions, said programming instructions not being operational until subsequent storing of said address table at the time of personalization; and

personalizing said IC card after said storing step by storing in said second memory said address table with memory addresses of at least one of said programming instructions;

wherein said operating system will only access [those] the programming instructions in accordance with the addresses indicated in the address table.

25. (Twice Amended) A secure multiple application card system including an IC card comprising a microprocessor, a read-only memory and an electrically erasable programmable read only memory, said system comprising:

means for manufacturing said IC card and for storing at the time of manufacture in said read-only memory an operating system and programming instructions, said programming instructions not being operational until subsequent storing of an address table with memory addresses of at least one of said programming instructions at the time of personalization; and

means for personalizing said IC card after the time of manufacture and for storing at the time of personalization in said electrically erasable programmable read only memory [an] said address table with memory addresses of at least one of said programming instructions,

wherein the operating system will only access [those] the programming instructions in accordance with the addresses indicated in the address table;

and wherein said means for personalizing said IC card can be operated to store additional programming instructions in said read-only memory and includes means for inserting addresses for said additional programming instructions in said address table.

33. (Twice Amended) A process for providing a secure multiple application card system including an IC card comprising a microprocessor, a read-only memory and an electrically erasable programmable read only memory, said process comprising the steps of:

manufacturing said IC card and storing at the time of manufacture in said read-only memory an operating system and programming instructions, said programming

instructions not being operational until subsequent storing of an address table with memory addresses of at least one of said programming instructions at the time of personalization;

personalizing said IC card after said time of manufacture by storing in said electrically erasable programmable read only memory [an] said address table with memory addresses of at least one of said programming instructions,

wherein the operating system will only access [those] the programming instructions in accordance with the addresses indicated in the address table;

storing additional programming instructions in said read-only memory; and

inserting addresses for said additional programming instructions in said address table.

39. (Twice Amended) A process for providing a secure multiple application card comprising a microprocessor, a first memory and a second memory, said process comprising the steps of:

a. storing in said first memory an operating system and programming instructions, said programming instructions not being operational until subsequent storing of an address table with memory addresses of at least one of said programming instructions at the time of personalization;

b. personalizing said IC card after said storing step by storing in said second memory [an] said address table with memory addresses of at least one of said programming instructions,

wherein said operating system will only access [those] the programming instructions in accordance with the addresses indicated in the address table;

c. storing additional programming instructions in said read-only memory; and

d. inserting addresses for said additional programming instructions in said address table.